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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHAND, ROBERTA A	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,465	ANNADURAI ET AL.	
	Examiner	Art Unit	
	Roberta A. Shand	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 9-17,20,21 and 24-28 is/are allowed.

6)☒ Claim(s) 1-8, 18, 19, 22, 23, 29-34 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4-8, 18, 19, 22, 23, 28-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura (U.S. 6385213 B1).

3. Regarding claims 1 and 8, Nakamura teaches (fig. 3) a method for detecting a boundary between two bytes X1 and X2 in a deserialized (abstract, parallel) data stream, the data stream comprising N consecutive X1 (A1) bytes followed by N consecutive X2 (A2) bytes, the method comprising the steps of: storing a first M bytes of data, where M is smaller than N; monitoring at least a subsequent second M bytes of data; comparing each of said first M bytes to a value X1*; comparing each of said second M bytes to a value X2*, wherein X1* represents X1 or any value resulting from a bit shift of X1 (A1), wherein X2* represents X2 or any value resulting from a bit shift of X2 (A2) (col. 10, lines 11-37), wherein the XIX2 boundary bytes (synchronous pattern)is detected (fig. 3, 14) when each of the first M bytes equals X1*, and each of said second M bytes equals X2*.

4. Regarding claim 2, Nakamua teaches (fig. 33, 16-1) the first M bytes are stored in a first data register.

5. Regarding claim 4, Nakamura teaches (col. 1, lines 10-20) the data stream is a portion of a SONET frame section header.

6. Regarding claims 5 and 6, Nakamura teaches (fig. 4 and col. 10) X1, X2 is the named byte A1, A2 in a SONET (SDH) frame section header.

7. Regarding claim 7, as for the SONET frame is an OC-N SONET frame, and wherein N represents the number of OC-1 frames multiplexed to form the OC-N frame, this is inherent in Nakamura's system since Nakamura teaches Sonet data.

8. Regarding claim 18. Nakamura teaches A SONET data processor comprising: a first register coupled to an input SONET data bus; a comparator (detection fig. 3) having at least a first input coupled to the input data bus and a second input coupled to the first register (fig. 10) such that the comparator has substantially simultaneous access to paralleled data associated with two successive clock cycles (fig. 10), wherein the comparator compares the values in some portion of the input data bus with a predetermined value, and wherein the comparator compares the values in some portion of the first register with a predetermined value (fig. 33).

9. Regarding claim 19, Nakamura teaches (fig. 18, 32a) a byte select bus outputted by said comparator whose value is determined by the difference between the values in some portion of the input and a predetermined value, and the difference between some portion of the first register with a predetermined value.

10. Regarding claims 22 and 23,. Nakamura teaches (figs. 28-30) the bit shifting circuit comprises an array of multiplexers.

11. Regarding claim 29. Nakamura teaches (fig. 3) a SONET (SDH) line card comprising: an optical transceiver coupled to receive an optical signal and to convert the optical signal to an electrical signal; an electrical transceiver coupled to receive the electrical signal and to deserialize (serial-to-parallel, S/P) the electrical signal into a plurality of parallel data streams; a framer coupled to the electrical transceiver and configured to detect an AIA2 (fig. 3, 14) boundary of the electrical signal; and a network processing unit coupled to the framer, wherein, the framer comprises the SONET (SDH) data processor of claim 18.

12. Regarding claims 30, 31 and 32, Nakamura teaches (fig. 6) a method of processing data in a SONET (SDH) frame, the method comprising: receiving first and second consecutive N bytes of data (m); comparing N/2 consecutive bytes of the first N bytes of data with a first predetermined pattern defined by the A1 byte in a SONET frame header (22); comparing N/2 consecutive bytes of the second N bytes of data with a second predetermined pattern defined by the A2 byte in a SONET frame header (23); if a match is found in both compare steps, forming a third consecutive N+1 bytes by combining the two N/2 consecutive bytes of data plus one additional byte; shifting data bits in each byte of the third consecutive N+1 bytes so that each byte corresponds to an A1 or an A2 byte (fig. 7); and shifting the A1 and M bytes to align N consecutive bytes along the AIA2 boundary (fig. 8).

13. Regarding claim 33. Nakamura teaches (fig. 8) the first predetermined pattern comprises the A1 pattern or any bit shifted version thereof.

14. Regarding claim 34, Nakamura teaches (fig. 8) the second predetermined pattern comprises the A2 pattern or any bit shifted version thereof

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura

17. Regarding claim 3, Nakamura does not explicitly teach the data register is a 128 bit It would have been obvious to one of ordinary skill in the art to adapt a 128 bit register to Nakamura as it is well known in the art.

18. Claims 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Soda (6359908 B1).

19. . Regarding claim 20, Nakamura does not teach the second data register stores the values stored in the first data register during a prior clock cycle.

20. Soda teaches (fig. 2) second register. It would have been obvious to one o ordinary skill in the art to adapt this to Nakamura's system to accommodate two bytes of data.

Allowable Subject Matter

21. Claims 9-17, 20, 21 and 24-28 are allowed.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberta A Shand whose telephone number is 571-272-3161. The examiner can normally be reached on M-F 9:00am-5:30pm.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Roberta A Shand
Examiner
Art Unit 2665

STEVEN NGUYEN
PRIMARY EXAMINER